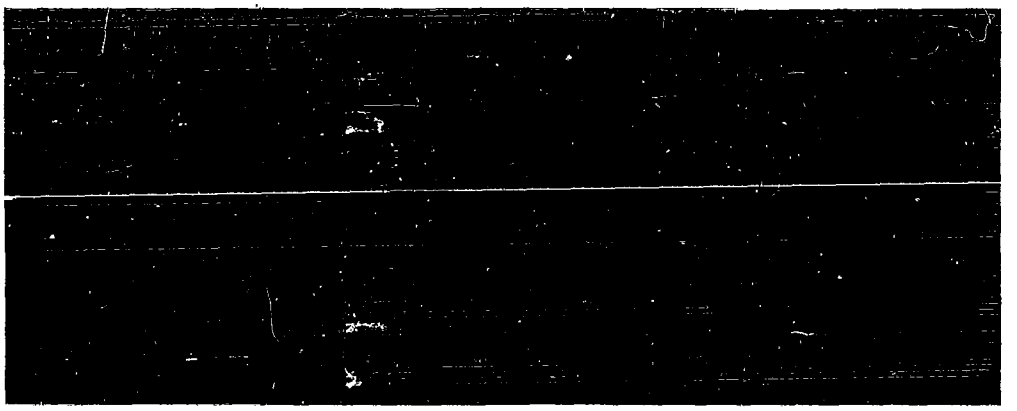


432477

Prepared By
R. Austin
G. Kamienski
P. Kellow
J. Logan
I. Massaron
R. San Vicente

Edited By
S. H. Barnes

U. S. Army Electronics Materiel Agency
Contract No. DA-36-039 SC-86742
Order No. 19064-PP-62-81-81

TRW SEMICONDUCTORS INC.
A SUBSIDIARY OF THOMPSON RAMO WOOLDRIDGE INC
14520 AVIATION BOULEVARD LAWNDALE CALIFORNIA

TRW SEMICONDUCTORS, INC.

Engineering Department
14520 Aviation Blvd.
Lawndale, California

Fifth Quarterly Report

PRODUCTION ENGINEERING MEASURE

Reliability Thru Process Improvement

(2N1506)

30 June 1963 to September 30, 1963

TRW Report No. 3000-43-Q-5

U. S. Army Electronics Materiel Agency Contract No. DA-36-039 SC-86742

Order No. 19064-PP-62-81-81

This contract calls for process improvement work and reliability evaluation to establish a failure rate for the 2N1506 transistor of 0.01% per thousand hours.

Prepared By

R. Austin, G. Kamienski, P. Kellow,
J. Logan, I. Massaron, R. San Vicente

Edited By

S. H. Barnes

Table of Contents

SECTION I - ABSTRACT

Conditions are ready for starting the production run. However, two areas, lead attachment and encapsulation, require additional engineering effort and shall continue to be investigated until the beginning of the production run.

Recent linear life test results are very encouraging and show low failure rate. The failures are being investigated and information utilized for additional process improvements.

SECTION II - PURPOSE

The purpose of this contract is to improve production techniques to increase the reliability for the 2N1506 Silicon Triple Diffused Transistor. A maximum operating failure rate of 0.01% per thousand hours at a 90% confidence level at 25°C shall be an objective. The process improvements specified below will be performed in attaining or exceeding the specified failure rate.

A. Material Evaluation

B. Impurity Diffusion

C. Contact Metallizing

D. Contact Lead Attachment

E. Collector Attachment

F. Final Preparation Prior to Sealing

G. Cap Welding

SECTION III - TECHNICAL DISCUSSION

CHAPTER I

Process Improvement

1.1 Introduction

During the last quarter most of the process evaluations have been concluded, and conditions established for the start of the production run. The purpose of the production run is to fabricate a given quantity of transistors to be placed on a 3000 hour life test to prove the attainment of a 0.01% per thousand hour failure rate.

Improvements made to date are summarized, followed by a description of the work accomplished during the fifth quarter. The areas of contact attachment and encapsulation have required additional effort. This effort will continue until the start of the production run.

1.2 Summary of Process Improvements Completed

1.2.1 Material Evaluation

Study of operational life failures has indicated that surface and not bulk has accounted for I_{CBO} and I_{EBO} failures. Failures after operating life were placed in a 200°C oven for twenty-four hours. These units showed a decrease in surface leakage to an acceptable low level. This process was repeated to verify the results. The 200 C bake activated the surface of the devices and a subsequent change between the surface and contacting material incurred. This phenomenon is characteristic of surface contaminations. A defect

in the bulk of the material can result in a leakage failure; however, a leakage failure due to bulk will not recover due to the damage caused by localized current density in the region of the defect.

1.2.2 Impurity Diffusion

The move of the diffusion production into the new clean room facility has been completed. New type diffusion furnaces have been incorporated into the production processes. Separate diffusion rooms for both P and N type operations have satisfied the planned requirements. The new diffusion furnaces are equipped with the laminar flow exhaust systems at the work ends, which minimize the impurity contamination within the working room areas.

Wet oxygen system has been established at mask oxidation to give a more pure and controllable process. Oxygen as the carrier gas is free of contamination, as opposed to room air in the steam system, contributing to a denser and cleaner oxide.

The glass mask photoresist process has presented some problems due to preparatory processes and soft emulsions. New masks with harder emulsions are under evaluation, whereby it is expected that film masks will be phased out of the process in time for the production run.

1.2.3 Collector Attachment

Evaluations of the semi-automatic bonding machine have given

negative results. Even though at times data was encouraging, lack of reproducible, consistent quality performance makes it necessary, at this time, to continue with the present mounting technique.

1.3 Process Evaluations In Progress

1.3.1 Contact Metallizing

This process is important in attaining 300 C storage capability without the problem of purple plague. The Au-Ni-In evaporated contact system has continued to be evaluated. The promising experimental results reported in the Fourth Quarterly Report led to a large scale evaluation to prepare for its adoption into the production processes. However, difficulties have been encountered in its adhesion consistency in large quantities of wafers, and a more detailed investigation into its production worthiness is under way.

1.3.2 Contact Lead Attachment

It has been determined that the most suitable bonder for fabricating the device is the nail-head bonder. A gold wire to gold metallizing system is the goal desired here. To attain this goal, two lead attachment methods are available. The first is gold wire wedge bonded. The second is gold wire nail-head bonded. An evaluation of mechanical strength was conducted to determine which system exhibited the strongest bonds. Six groups (average size 14 devices per group) were subjected to an 11 grams pull test. If the bond or wire failed, the lead wire

was considered unacceptable. Nearly 50% of all the nail-bond devices exceeded the 11 gram pull test, while only one group of the wedge bonded units yielded 50%. These tests indicated the nail-head bonder to be most suitable bonder for fabricating this device utilizing the gold wire to gold metallizing system.

1.3.3 Final Preparation Prior to Sealing

The experiments on molecular sieve have been confirmed and results indicate no failures for either the experimental or control lots.

It can be stated with a confidence level of 90% at this time that the elimination of the sieve does not have detremental effects on device reliability. In fact, the elimination of sieve is considered to decrease the probability of failure that might occur because of loose particles that may become detached from the sieve buffer, or retainer ring.

Other evaluations relating to cleaning and vacuum baking requirements continue. Failure analyses indicate that the preparation of the device prior to cap welding is critical and is a factor in reliability of the device.

1.3.4 Cap Welding

Evaluations now in progress are designed toward elimination of the hot nitrogen flush, and incorporating in its place a room temperature dry nitrogen atmosphere for capping through the use of a dry box system. The units will then exit from the high vacuum bake process into the dry box where the cap welding operation will take place

CHAPTER 2

RELIABILITY TESTING AND EVALUATION

P. Kellow and J. Logan

2.1 Introduction

During this quarter, a technical draft, TAR No. 1, has been completed and submitted to the Commanding Officer, U. S. Army Electronics Materiel Agency, Fort Monmouth, New Jersey, covering an Objective Specification for the 2N1506 transistor. This specification provides the reliability requirements for the transistor that has been developed as a result of this program and also indicates the estimated failure rate for the final production run presently to be commenced.

Two engineering experiments were submitted during the quarter for reliability evaluation that comprise a partial portion of the final phase of the engineering improvement work.

One experiment was to determine the associated incidence of surface and bonding degradation (purple plague) at step-stress storage temperatures after controlled process variations had been introduced. This experiment was evaluated as lot number 633441.

The second experiment, Lot 633811, was conducted to confirm previous investigations dealing with variable gaseous atmospheres during the transistor encapsulation operation.

In addition to these two experiments, an impact shock test series

was performed to evaluate internal lead attachment and dice contact to the transistor header. This was lot 633442.

The final portion of this chapter summarizes the failure rates realized during the quarter from the evaluation of standard production lots following operating and storage life tests.

2.2 Experiment Evaluation - Bonding Investigation

Lot number 633441 consisted of forty-three (43) transistors that had been fabricated using aluminum metallizing, gold internal lead wires and active element connection by means of nailhead thermocompression bonding.

The test evaluation model was established to provide a ready comparison of cumulative percent failure to a control lot (631151) that had been previously tested under similar conditions with the exception that the +325°C step was eliminated for this present test.

The test conditions, end point characteristics, characteristic failures and a comparison failure chart are listed in Tables 2.1 through 2.5.

Table 2.1, Test Conditions for Lot 633441

Stress	Temperature	Time at Stress Level	Cumulative Test Time
S_1	+225°C	24 hrs.	24 hrs.
S_2	+250°C	24 hrs.	48 hrs.
S_3	+275°C	24 hrs.	72 hrs.
S_4	+300°C	24 hrs.	96 hrs.

Temperature tolerance was held to ± 3°C. Time tolerance was within the stated period $\pm \frac{4}{0}$ hrs.

Prior to submission of the transistors to test, zero hour characteristics were read as in Table 2.2. At the completion of each 24 hour test step, the transistors were removed from the test environment and allowed to stabilize for 4 hours, ± 30 minutes, at an ambient temperature of +25°C before end point characteristics were read.

Table 2.2, End Point Characteristics for Lot 633441

Characteristic	Conditions	Limits
I_{CBO}	V_{CB} = 28V DC	≤ 10μA
I_{EBO}	V_{CE} = 4V DC	≤ 100μA
BV_{EBO}	I_E = 100 μA	≥ 4V DC

Table 2.3, Characteristic Failures of Lot 633441

Stress Temperature	Number Defective	Characteristic Defective	Cumulative Percent Failure
+225°C	1	I_{CBO}	2.4%
+250°C	23	I_{EBO}	57.0%
+275°C	6	I_{EBO}	71.0%
+300°C	7	I_{EBO}	88.0%

The critical temperature lies between +225°C and +250°C since an excess of 50% of the test lot failed after the +250°C step. As compared to control lot 631151 run during the first quarter of this year, the incidence of failure is significantly higher.

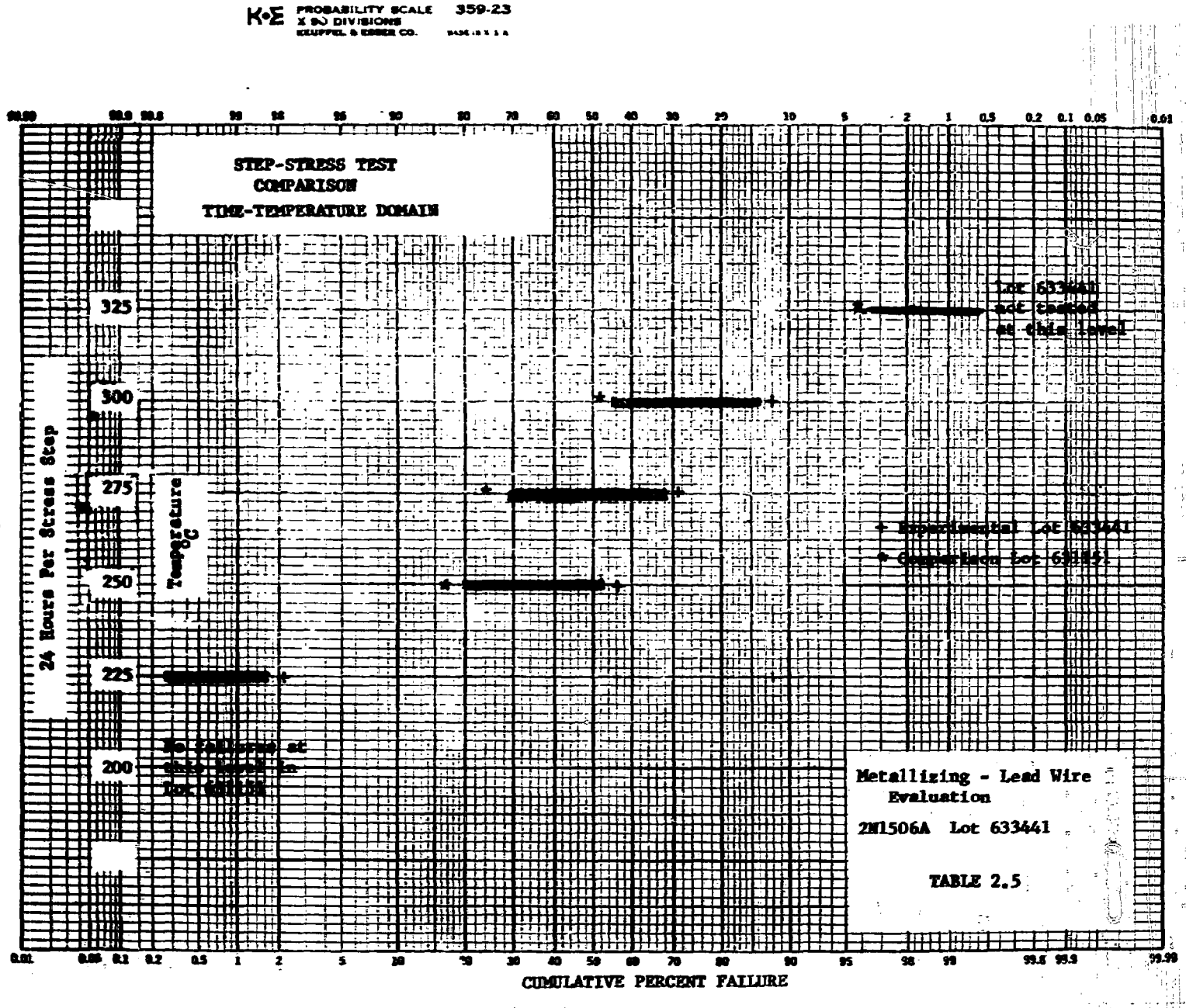
Table 2.4, Characteristic Failures of Lot 631151

Stress Temperature	Cumulative Percent Failures				
	T_1	T_2	T_3	T_4	T_5
+225°C	0				
+250°C		17%			
+275°C			25%		
+300°C				50%	
+325°C					96%

The transistors comprising the control lot had been randomly selected from production material and run as control group for an experimental lot on special metallizing. See PSI Report No. 3000-43-Q-3, page 23.

As shown by the comparison table (Table 2.5), the experimental process utilized in lot 633441 is not superior to the standard production lot ran early this year.

It is highly probable, however, that some unknown process variables have entered into the experiment evaluation to preclude its optimum utilization of assessing the experimental technique. But, since the experimental transistors have not as yet been completely analyzed by Engineering to determine the failure cause, it is difficult to make any definitive statement at this time with any degree of certainty.


K•E PROBABILITY SCALE 359-23
X BY DIVISIONS
KEUFFEL & ESSER CO.
STEP-STRESS TEST
COMPARISON
TIME-TEMPERATURE DOMAIN
325
300
275
250
225
200
24 Hours Per Stress Step
Temperature °C
Lot 633441 not tested at this level
+ Experimental Lot 633441
+ Comparison Lot 633441
No failures at this level in Lot 633441
Metallizing - Lead Wire Evaluation
2N1506A Lot 633441
TABLE 2.5
99.99 99.9 99.8 99 98 95 90 80 70 60 50 40 30 20 10 5 2 1 0.5 0.2 0.1 0.05 0.01
CUMULATIVE PERCENT FAILURE

The major and most often repeated failure mode remains to be a degradation of the emitter-base junction and the surface passivation layer, as indicated by test data and preliminary physical failure analysis.

2.3 Experiment Evaluation - Encapsulation

Lot 633811 was submitted for evaluation to determine if variation of gaseous atmosphere during encapsulation would have any significant effect upon transistor failure during power operation.

A sample of twenty-five (25) transistors were selected from both the experimental and control groups and subjected to power step-stress as in the following table.

Table 2.6, Test Conditions for Lot 633811

Stress	Operating Conditions V_{CB}	I_C	Power Level Watts	Percent Rated Power	Time at Stress Level	Cumulative Test Time
S_1	20V	40MA	0.8W	100%	24 hrs.	24 hrs.
S_2	20V	60MA	1.2W	150%	24 hrs.	48 hrs.
S_3	20V	80MA	1.6W	200%	24 hrs.	72 hrs.
S_4	20V	100MA	2.0W	250%	24 hrs.	96 hrs.
S_5	20V	120MA	2.4W	300%	24 hrs.	120 hrs.

The end-point characteristics were the same for this lot as for lot 633441 as indicated in Table 2.2.

Approximately ninty (90) transistors each comprised the experimental and control groups submitted to operating life test at 0.8W with conditions as S_1 above for 1000 hours. Since the experimental lot was submitted just recently, only 500 individual test hours have been accrued to date.

In Table 2.7, the cumulative percent failures are listed following the power step-stress test.

Table 2.7, Cumulative Percent Failures for Lot 633811, Group A and Group B

Test Group	Cumulative Percent Failure At Stress Power Level in Watts				
	0.8W	1.2W	1.6W	2.0W	2.4W
Group A Experiment	0	0	60%	80%	96%
Group B Control	0	0	60%	84%	96%

As indicated in the table, the power step-stress test does not reveal any significant difference in the occurrance of failures as a result of the experimental technique compared to the control group.

2.4 Impact Shock Evaluation

The purpose of this evaluation was to determine the failure threshold of standard production transistors when subjected to impact shock in cumulatively increasing G levels.

The test was conducted according to MIL-STD-750, Method 2016, with the exception that shock exposure was limited to the Y_1 orientation only.

The G force was applied in five blows for about 0.22 milliseconds each at 4000, 6000, 8000, 9000, and 10,000 G's per step. One additional step of 11,000 G's is presently in process.

At the completion of each step, the cumulative effect of the impact shock was analysed by testing pre-selected characteristics.

The analysis of the characteristic test data indicated that the transistors were not greatly affected by the impact shock. No physical damage was experienced at any impact level.

There was a slight shift noted in the variance about the mean of the characteristic distributions, but no out of limit conditions existed. The characteristics and limits are the same as in Table 2.2.

In reviewing the results of this test series and also the cumulative constant acceleration test series concluded last year, it can be stated with some considerable certainty that the drop shock screening test submitted to all manufactured product is most effective in removing potentially weak transistors.

These two test series have verified that the drop-shock test will guarantee transistors capable of withstanding at least 10,000 G's of impact shock and at least 40,000 G's constant acceleration.

2.5 Linear Life Test

The following, Table 2.8, summarizes the standard production lots evaluated during this last quarter.

Samples from standard lots were selected and placed on operating life at 0.8W (V_{CB} = 20V, I_C = 40MA) and non-operating storage life at +200°C for 1000 individual transistor hours.

End-point characteristics were as in Table 2.2 with end-point intervals at 100, 250, 500, and 1000 hours. Prior to each end-point test, the samples were stabilized at +25°C ambient for four hours ± 30 minutes.

All lots tested include the latest process improvements that have been implemented by Engineering.

The failed transistors have been submitted to Engineering for complete physical failure analysis and investigation for process corrective action.

Table 2.8, Linear Life Test - Operating and Storage Life

Lot Number	Test Performed	Qty. Tested	Failure Occurrance 100	250	500	1000	Total Transistor Test Hours	Failure Rate %/1000 Hours
A1503-05	Operating Life	89	0	2 I_{CBO}	2 I_{CBO}	6 I_{CBO}	83,350	12.0%
A1503-06	Operating Life	50	0	0	0	0	50,000	0
A1503-07	Operating Life	50	0	0	1 short	Test not complete		
A1503-08	Operating Life	50	0	0	0	Test not complete		
A1503-05	Storage Life	88	0	1 short	0	2 I_{CBO}	87,657	3.4%
A1503-06	Storage Life	50	0	0	0	2 V_{EBO}	49,500	4.0%
A1503-07	Storage Life	50	0	0	0	Test not complete		
A1503-08	Storage Life	50	0	0	0	Test not complete		

SECTION IV

SUMMARY AND CONCLUSIONS

Most process improvements have been completed. The changes in production facilities have been incorporated in the line with the resultant improvement in the diffusion areas.

Additional effort has been devoted to lead attachment and encapsulating processes. The evaluations in these areas will continue until the start of the production run.

Recent linear life test results are very encouraging and show low failure rates. The failures are being investigated and information utilized for additional process improvements.

Issuance of final processes and flow charts is being delayed in order to incorporate all the improvements prior to the production runs.

SECTION V

PUBLICATIONS, REPORTS AND CONFERENCES

There have been no publications, reports or conferences during the fifth quarter.

SECTION VI

EXPENDITURES

Professional labor which was expended during the contract period was as follows:

	Hours
S. H. Barnes	19
R. San Vicente	312
J. K. Logan	11
D. Kliem	343
R. Logan	127
I. Massaron	136
H. A. Paschal	192
P. Kellow	23
K. Pierick	13
Total	1176 hours

Technical effort during the period amounted to 1,142 hours.

UNCLASSIFIED